| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/466,405 | 12/17/1999 | FARRELL L. OSTLER | PHA23.891 | 1131 |

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| EXAMINER |
|---|
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| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | 7 |

DATE MAILED: 05/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 07-01)

**-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on _24 April 2003_ .

2a)☒ This action is **FINAL**.　　　2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under _Ex parte Quayle_, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) _1-9_ is/are pending in the application.

　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-9_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _17 December 1999_ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

　　If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☐ All b)☐ Some * c)☐ None of:

　　　1.☐ Certified copies of the priority documents have been received.

　　　2.☐ Certified copies of the priority documents have been received in Application No. _____ .

　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
　　　　application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

　　a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .

4)☐ Interview Summary (PTO-413) Paper No(s). _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____ .

# DETAILED ACTION

## *Drawings*

1.      The drawings are objected to under 37 CFR 1.83(a).  The drawings must show every

feature of the invention specified in the claims.  Therefore the default register must be shown in

the drawings or the feature cancelled from the claims.  Furthermore, the method claims must be

shown in the drawings, for example in a flow chart, or the feature(s) canceled from the claim(s).

No new matter should be entered.

*2.*      A proposed drawing correction or corrected drawings are required in reply to the Office

action to avoid abandonment of the application.  The objection to the drawings will not be held

in abeyance.

## *Claim Rejections - 35 USC § 112*

3.      The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making
> and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it
> pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode
> contemplated by the inventor of carrying out his invention.

4.      Claims 1-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with

the enablement requirement.  The claim(s) contains subject matter which was not described in

the specification in such a way as to enable one skilled in the art to which it pertains, or with

which it is most nearly connected, to make and/or use the invention.  The limitation in claim 1,

"A first instruction that is configured to cause the processor to *concurrently* load a specified

address into the default register to form the default destination address and execute program

instructions that are located in the memory at the default-destination address contained in the

default register" is not enabled by the specification.  Instead, the specification discloses a default

register, a first instruction to load a specified address into the default register, and a second

instruction to execute program instructions that are located in the memory at the default-

destination address contained in the default register. The specification does not disclose that the

second instruction is concurrently executed with the first instruction as claimed in claim 1.

Therefore, for purposes of examination, the limitation "A first instruction that is configured to

cause the processor to *concurrently* load a specified address into the default register to form the

default destination address and execute program instructions that are located in the memory at

the default-destination address contained in the default register" is interpreted as being a first

instruction to load a specified address into the default register, and a second instruction, which is

not concurrently executed with the first instruction, to execute program instructions that are

located in the memory at the default-destination address contained in the default register.

5.      Independent claims 6 and 7 contain the same defects of independent claim 1 and are

therefore rejected for the same reasons of claim 1.

6.      Claim 2-5, 8, and 9 are rejected for incorporated the defects of their depending claims 1,

6, and 7.

## *Claim Rejections - 35 USC § 102*

7.      The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8.      Claims 1-9 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Davidson

et al., cited by Applicant in the Information Disclosure Statement filed on August 2, 2001.

9.      Referring to claim 1, Davidson et al have taught a processor that is configured to execute

program instructions that are stored in a memory, said processor comprising:

        a.      a default-register that is configured to contain a default-destination address

(abstract, page 183, section 3, "The branch Register Approach", page 184, see

"Conditional Branches", and see b[7] in the example code.); and

        b.      wherein the program instructions include:

                i.      a first instruction that is configured to cause the processor to concurrently

        load a specified address into the default-register to form the

        default-destination-address and execute program instructions that are located in

        the memory at the default destination-address contained in the default-register

        (page 184, "Conditional Branches", b[7] = r[5] < 0 - > b[2] | b[0]; is the first

        instruction which loads an address into the default register b[7]. This first

        instruction later causes the processor to execute program instructions at the

        default destination address contained in the default-register when the value of b[7]

        is loaded into b[0].), and

                ii.     a second instruction that is configured to cause the processor to

        subsequently execute the program instructions that are located in the memory at

        the default-destination-address contained in the default-register (pages 184,

        "Conditional Branches", b[0] = b[7]; is the second instruction that is executing

        instructions located in memory at the default-destination-address contained in the

        default-register, b[7].).

10.    Referring to claim 2, Davidson et al. have taught the processor of claim 1, as described

above, and wherein the second instruction includes a condition test and is further configured to

cause the processor to execute program instructions that are located at the

default-destination-address in dependence upon a result of the condition test (pages 184,

"Conditional Branches", When executing the second instruction, or b[0] = b[7];, the value loaded

into b[0] is dependent on the condition test value b[7].).

11.    Referring to claim 3, Davidson et al. have taught the processor of claim 1, as described

above, and wherein the default-register is further configured to

    a.    contain a default condition-test (pages 184, "Conditional Branches", When

    executing the second instruction, or  b[0] = b[7]; , the value loaded into b[0] is dependent

    on a default condition test value b[7], which was derived in another instruction, or b[7] =

    r[5] < 0  - >  b[2] | b[0];.); and

    b.    wherein the second instruction is further configured to cause the processor to

    execute program instructions that are located at the default-destination-address in

    dependence upon a result of the default-condition-test contained in the default-register

    (pages 184, "Conditional Branches",  When executing the second instruction, or b[0] =

    b[7]; , the value loaded into b[0] is dependent on a default condition test b[7].).

12.    Referring to claim 4, Davidson et al. have taught the processor of claim 1, as described

above, and wherein the second instruction is further configured to cause the processor to execute

program instructions that are located at the default-destination-address in dependence upon a

result of a prior condition-test (pages 184, "Conditional Branches", When executing the second

instruction, or b[0] = b[7]; , the value loaded into b[0] is dependent on the result in b[7] derived

in a prior condition-test, or in b[7] = r[5] < 0  - >  b[2] | b[0];.).

13.     Referring to claim 5, Davidson et al. have taught the processor of claim 1, as described

above, and wherein

a.      the default-register is further configured to contain a default condition-test (page

184, see "Conditional Branches", in the example code, b[7] = r[5] < 0  - >  b[2] | b[0];

the branch register b[7] is set based on the value of r[5].  b[7] is the result of the test, or

the default condition-test.); and

b.      wherein the program instructions further include:

i.      a third instruction that is configured to cause the processor to execute

program instructions that are located at another specified address in dependence

upon a result of the default-condition-test contained in the default-register (page

184, see "Conditional Branches", in the example code  the branch register is set

based on the value of r[5].  Based on the value of r[5], b[2] or b[0], which is

another specified address, is loaded into b[7].).

14.     Referring to claim 6, Davidson et al. have taught a processor that is configured to execute

program instructions that are stored in a memory (Figure 1, Instructions are fetched from the

cache memory.), said processor comprising:

a.      a default-register that is configured to contain a default-condition-test (abstract,

page 183, section 3, "The branch Register Approach", page 184, see "Conditional

Branches", and see b[7] in the example code.); and

b.      wherein the program instructions include:

      i.     a first instruction that is configured to cause the processor to concurrently

load a specified condition into the default-register to form the

default-condition-test and execute program instructions that are located in the

memory at a destination-address based on a result of the default-condition-test

(page 184, "Conditional Branches", b[7] = r[5] < 0 -> b[2] | b[0]; is the first

instruction which loads an address into the default register b[7]. This first

instruction later causes the processor to execute program instructions at the

default destination address contained in the default-register when the value of b[7]

is loaded into b[0].), and

      ii.     a second instruction that is configured to cause the processor to

subsequently execute program instructions that are located in the memory at a

destination-address based on a result of the default-condition-test (pages 184,

"Conditional Branches", When executing the second instruction, or b[0] = b[7]; ,

the value loaded into b[0] is based on a result of a condition test, or b[7] = r[5] < 0

-> b[2] | b[0];.).

15.     Referring to claim 7, Davidson et al. have taught a method of controlling a sequence of

program instructions, said method comprising:

      a.     executing a first instruction that concurrently specifies a destination address and

conditionally causes the default-destination address to become a next instruction address

during, a first processing cycle (page 184, "Conditional Branches", b[7] = r[5] < 0 ->

b[2] | b[0]; is the first instruction which loads an address into the default register b[7].

This first instruction later causes the processor to execute program instructions at the

default destination address contained in the default-register when the value of b[7] is

loaded into b[0].);

b.        subsequent to an execution of the first instruction, executing a second instruction

that causes the default-destination-address to become the next instruction address during

a second processing cycle (pages 184, "Conditional Branches", b[0] = b[7]; is the second

instruction that causes the default-destination-address to become the next instruction

address during a second processing cycle.); and

c.        subsequent to an execution of the second instruction, executing a third instruction

that is located at the next instruction address (pages 184, "Conditional Branches", L2: ...

, The instruction located at L2, or the next instruction address, is the 3$^{rd}$ instruction

executed.).

16.       Referring to claim 8, Davidson et al. have taught the method of claim 7, as described

above, and further comprising:

a.        executing a fourth instruction, before executing the second instruction, that

specifies a condition-test (page 184, "Conditional Branches", b[7] = r[5] < 0  -> b[2] |

b[0]; is the fourth instruction which is executed before the second instruction, b[0] =

b[7];.   The value of r[5] is the condition being tested and b[7] contains the result or

condition test.); and

b.        wherein causing the default-destination-address to become the next instruction

address during the second processing cycle is dependent upon a result of the

condition-test when the second instruction is executed (page 184, "Conditional

Branches", When executing the second instruction, or  b[0] = b[7]; , the value loaded into

b[0] is dependent on the condition test in the fourth instruction, or b[7] = r[5] < 0 - >

b[2] | b[0];.).

17.      Referring to claim 9, Davidson et al. have taught the method of claim 7, as described

above, and further comprising:

a.      saving a result of a condition-test, before executing the second instruction (page

184, "Conditional Branches", b[7] = r[5] < 0 - > b[2] | b[0]; , The result of the condition

test is saved in b[7] before executing the second instruction, b[0] = b[7].); and

b.      wherein causing the default-destination-address to become the next instruction

address during the second processing cycle when executing the second instruction is

dependent upon the result of the condition-test (page 184, "Conditional Branches", When

executing the second instruction, or b[0] = b[7]; , the value loaded into b[0] is dependent

on the result of a condition test, or b[7] = r[5] < 0 - > b[2] | b[0];.).

### *Response to Arguments*

*18.*      Applicant's arguments with respect to claims 1-9 have been considered but are moot in

view of the new ground(s) of rejection.

### *Conclusion*

19.      Applicant's amendment necessitated the new ground(s) of rejection presented in this

Office action.  Accordingly, **THIS ACTION IS MADE FINAL**.  See MPEP § 706.07(a).

Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

20.      A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action.  In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this

final action.

21.     Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993.

The examiner can normally be reached on Monday-Friday, 9-6:30, with every other Friday off.

22.     If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 746-7239 for regular

communications and (703) 746-7238 for After Final communications.

23.     Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is (703) 305-3900.

tlm
May 12, 2003

RICHARD L. ELLIS
PRIMARY EXAMINER